In the claims:

For the Examiner's convenience, all pending claims are presented below with

changes shown in accordance with the mandatory amendment format.

1.   (Currently Amended) A method of translating instructions, said method

comprising:

translating a first block of instructions executable in a first processor architecture,

into a translated first block of instructions executable in a second processor architecture,

said translated first block of instructions operating with a stack of data entry positions;

and

during the translating, generating an expected Top of Stack (TOS) position in said

stack for said first block of instructions ~~code~~; and

during the translating, adding at least one instruction to said translated first block

of instructions to determine if said first expected TOS is equal to an actual TOS position

in said stack at a time of executing said translated first block of instructions;

wherein said at least one instruction branches to correction code if said expected

TOS is not equal to said actual TOS, and

wherein said correction code to generate a delta of said expected TOS and said

actual TOS and to adjust said stack for said first block of instructions by the delta at the

time of executing said translated first block of instructions.

2.   (Canceled)

3.   (Canceled).

Docket No.: 042390.P7512
Application No.: 09/676,175   2

4.   (Currently Amended) The method as claimed in claim 1 [[3]], said·method further comprising:

    determining if execution of instructions in said first block of instructions changes the actual TOS.

5.   (Currently Amended) The method as claimed in claim 4, said method further . comprising:

    in response to determining execution of instructions in said first block of instructions changes the actual TOS, adding an instruction to an end of the first block of instructions to update the actual [[to]] TOS.

6.   (Currently Amended) A computer-readable medium having stored thereon a set of instructions to translate instructions, said set of instructions, which when executed by a processor, cause said processor to perform a method comprising:

    translating a first block of instructions executable in a first processor architecture, into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions;

    during the translating, generating an expected Top of Stack (TOS) position in said stack for said first block of instructions eode; and

    during the translating, adding at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS at a time of executing said translated first block of instructions;

Docket No.: 042390.P7512
Application No.: 09/676,175   3

wherein said at least one instruction branches to correction code if said expected

TOS is not equal to said actual TOS, and

wherein said correction code to generate a delta of said expected TOS and said

actual TOS and to adjust said stack for said first block of instructions by the delta at the

time of executing said translated first block of instructions.

7.   (Canceled)

8.   (Canceled).

9.   (Currently Amended) The computer-readable medium as claimed in claim 6 [[8]],

wherein said set of instructions further includes additional instructions, which when

executed by said processor, cause said processor to perform said method further

comprising:

determining if execution of instructions in said first block of instructions changes

the actual TOS.

10.   (Currently Amended) The computer-readable medium as claimed in claim 9,

wherein said set of instructions further includes additional instructions, which when

executed by said processor, cause said processor to perform said method further

comprising:

Docket No.: 042390.P7512
Application No.: 09/676,175   4

in response to determining execution of instructions in said first block of

instructions changes the actual TOS, adding an instruction to an end of the first block of

instructions to update the actual [[to]] TOS.

11.   (Previously Presented) A system comprising:

a first unit of logic to translate a first block of instructions executable in a first

processor architecture, into a translated first block of instructions executable in a second

processor architecture, said translated first block of instructions operating with a stack of

data entry positions; and

a second unit of logic to generate an expected Top of Stack (TOS) position in said

stack for said first block of instructions ~~code~~, wherein said second unit of logic further

adds at least one instruction to said translated first block of instructions to determine if

said first expected TOS is equal to an actual TOS at a time of executing said translated

first block of instructions;

wherein said at least one instruction branches to correction code if said expected

TOS is not equal to said actual TOS, and

wherein said correction code to generate a delta of said expected TOS and said

actual TOS and to adjust said stack for said first block of instructions by the delta at the

time of executing said translated first block of instructions.

12.   (Canceled)

13.   (Canceled).

Docket No.: 042390.P7512
Application No.: 09/676,175   5

14.   (Currently Amended) The system as claimed in claim 11 [[13]], wherein said

second unit of logic determines if execution of instructions in said first block of

instructions changes the actual TOS.

15.   (Currently Amended) The system as claimed in claim 14, wherein said second

unit of logic, in response to determining execution of instructions in said first block of

instructions changes the actual TOS, adds an instruction to an end of the first block of

instructions to update the actual [[to]] TOS.

16.   (New) The method as claimed in claim 1, wherein to adjust said stack for said

first block of code by the delta includes rotating said stack by the delta.

17.   (New) The computer-readable medium as claimed in claim 6, wherein to adjust

said stack for said first block of code by the delta includes rotating said stack by the delta.

18.   (New) The system as claimed in claim 11, wherein to adjust said stack for said

first block of code by the delta includes rotating said stack by the delta.

19.   (New) The method as claimed in claim 5, wherein to update the actual TOS

results in an expected TOS corresponding to a second block of instructions matching the

actual TOS, said second block of instructions following said first block of instructions in

execution and further operating with said stack.

Docket No.: 042390.P7512
Application No.: 09/676,175   6

20.   (New) The computer-readable medium as claimed in claim 10, wherein to update

the actual TOS results in an expected TOS corresponding to a second block of

instructions matching the actual TOS, said second block of instructions following said

first block of instructions in execution and further operating with said stack.

21.   (New) The system as claimed in claim 15, wherein to update the actual TOS

results in an expected TOS corresponding to a second block of instructions matching the

actual TOS, said second block of instructions following said first block of instructions in

execution and further operating with said stack.

Docket No.: 042390.P7512
Application No.: 09/676,175   7